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A method for qualitatively determining the depth position of a single atom in a nanometer scale field effect device structure

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Abstract

This work reports on a method for detecting the vertical depth position of single atom in a nanometer scale semiconductor field effect device at cryogenic temperature. The depth position is qualitatively obtained from the analysis of the acceptor-to-gate capacitances.

1. Introduction:

Over the last decade the interest in nanoscale devices has increased. This is because devices at nanometer scale levels are important for both fundamental Physics and applications. For example, experiments [1] have shown that electrons trapped in a quantum dot device occupy quantized energy levels similar to that of natural atoms. This opens a new method for studying the atomic spectra using laboratory fabricated quantum dots. Quantum dots can be used to form the basic logic circuits for future quantum information technology. However, with current advancement in nanofabrication techniques, it becomes possible to realize devices with single natural atoms [2]. This stimulates proposals where single natural atoms replace quantum dots and act as functional parts of the devices. This requires full controllability and manipulation of the spin and charge states in single atoms. It is also important to identify the position of these atoms in nanoscale devices.

Here we report on a method for detecting the vertical depth position of single atom in a nanometer scale semiconductor field effect device.

2. Device structure

Figure 1a shows schematic of the device consisting of top gate electrode (top gate voltage, V_U) and back gate electrode (back gate voltage, V_B). The electric field from the gates controls the electron current flowing between the right and left electrode across the semiconductor region. Silicon is a typical semiconductor used in the fabrication of such structures (e.g., MOSFET) [3]. The gates are isolated from the semiconductor by the insulators which are, for example, thermally grown silicon oxides. V_R and V_L are the voltages at the right and left electrodes, respectively.

Visible (Fig. 1a) is a single atom inside the semiconductor. The atom is located at depth d from the front surface (or interface) between the semiconductor and the upper insulator. Single atom can be realized by bombarding or implanting the surface of the semiconductor with atoms at low concentration such that the mean number of atoms in a nanometer scale region is about one atom. For example, it has been shown that [4, -5] a concentration of 1×10^{17} atoms/cm^3 gives rise to about 1 atom in the region with width L = 40 nm (Fig. 1a).

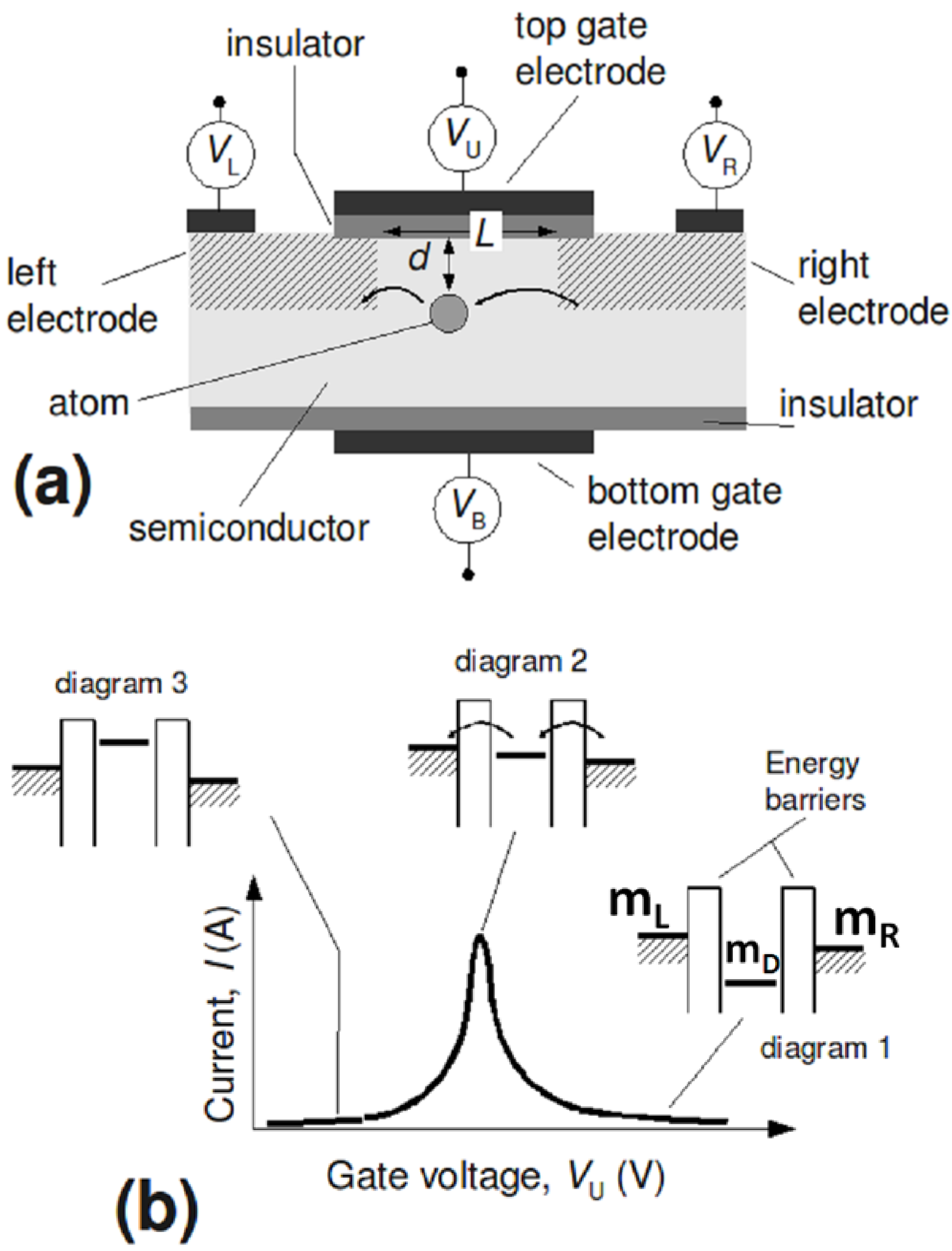

Figure 1 (a) nanoscale field effect device structure (b) energy levels (m_D, m_L and m_R) at a tunneling current peak.

3. Electron tunnelling through the atom:

The current I versus the upper gate voltage V_U is illustrated schematically in Fig. 1b for fixed values of V_B, V_L, and V_R. The current pattern has a peak structure with nearly zero current at both sides of the peak. The origin of the current peak structure is discussed with the aid of the energy band diagrams (diagram 1, 2, and 3, top of Fig. 1b). In diagram 1 the ground state energy level is assigned m_D which is coupled to (or interacting with) the energy levels (or Fermi levels) m_R and m_L of the metallic electrons (or electron sea) at the side electrodes through the simplified rectangular energy barriers. These barriers allow electron tunnelling between the atom and the electrodes as indicated by the curved arrows in diagram 2 and in Fig. 1(a), giving rise to the current peak. The energy barriers are either formed by the resistance of the semiconductor region or by the bending in the conduction band (as suggested by Poisson equation [3]) due to the change in the electron concentration from the atom to the electrode across the semiconductor.

We consider the case where V_R nearly equals 0 V (i.e, equilibrium transport regime) and V_L is slightly larger than V_R such that the energy levels at the electrodes satisfy: m_R (= eV_R) is slightly larger than m_L (= eV_L), where e is the negative charge of the electron. The condition for sequential electron tunneling between the electrodes across the atom is $m_R > m_D > m_L$.

The electric field from the gate voltage V_U is used to move the level m_D up and down through the energy window between m_R and m_L. For example, in the V_U range indicated by diagram 1 (Fig. 1b) the tunnelling condition is not satisfied and, hence, the current is zero because $m_D < m_L$. Sweeping V_U from right to left (i.e. reducing V_U) in Fig. 1b shifts m_D up towards m_R and m_L until the tunnelling condition $m_R > m_D > m_L$ is satisfied as shown in diagram 2. Here the tunnelling current (curved arrows, diagram 2 and Fig. 1a) reaches its maximum at the peak. As V_U is further reduced, m_D moves above m_R and m_L and the current drops to zero as indicated by diagram 3 in Fig. 1b. The second electron tunnelling is blocked (Coulomb blockade phenomena [6]) due to the electron-electron electrostatic repulsion.

4. Surface current

At large V_U values, electrons (hatched region, Fig. 2a) are attracted by the gate electric field towards the upper surface of the semiconductor near the top oxide as shown in Fig. 2a. In this case the surface resistance is reduced (recall that resistivity is proportional to electron concentration) and the current increases. The sharp rising current in Fig. 2b after the tunnelling current peak is the current flowing at the surface (i.e., the surface current).

5. Identification of depth position

Here we describe a method for qualitatively identifying the depth position, d (Fig. 1a), of the atom from the shift of the tunnelling peak (Fig. 2b) as we change both V_U and V_B voltages at fixed small V_L and V_R values. We will discuss three depth positions for the atom; near the front surface, near the back surface, and near the middle of the semiconductor. We will only focus on the tunnelling current peaks while neglecting the surface current.

5.1 Front atom

The top-right of Fig. 3 shows an atom near the front surface at large V_B and small V_F such that the electrons are attracted towards the back surface, forming a layer of electrons (hatched region) indicated as back electron layer in Fig. 3. Because the electron layer with large enough concentration of electrons acts as a conducting sheet, it cannot be penetrated by electric field [7] from the back gate. In other words the inner part of the semiconductor is screened from the back gate electric field by the back layer of electrons. This means that the atom near the front surface cannot feel the electric field from the back gate. So changing V_B will not affect m_D. Consequently the atomic level m_D can only respond to

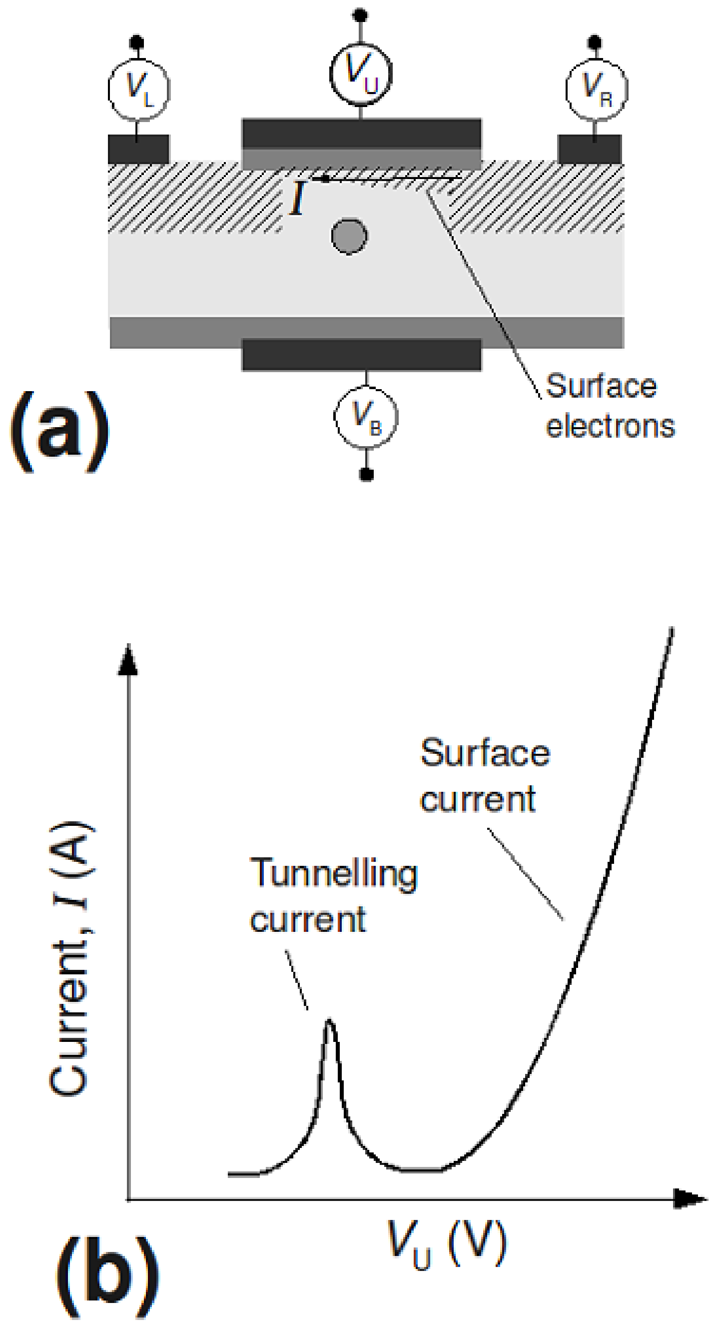

Figure 2 (a) schematics of the surface current I through the front interface electronic layer in a field effect nanodevice. (b) The current (surface plus tunneling) versus the gate voltage in a nano-field effect device with single atom.

changes in V_U. This case can be visualized by plotting the current peak, which is related to m_D as we discussed in the section 3, versus V_B (vertical axis) and V_U (horizontal axis) as shown by the dotted line in the bottom-right of Fig. 3. From this kind of plot the strength of coupling (or interaction) between the atom and the gates can be expressed by the ratio C_U/C_B [1], where C_B is the capacitance [7] between the back gate and the atom, and C_U is the capacitance between the upper gate and the atom. These capacitances quantify the strength of coupling between the gates and the atom; the larger the capacitance the stronger is the coupling. The capacitance ratio is given by $C_U/C_B = \Delta V_B/\Delta V_U$ where $\Delta V_B/\Delta V_U$ = the slope of the peaks line in bottom-right of Fig. 3, ΔV_B is the shift of the peak line along the V_B axis, and ΔV_U is the shift along the V_U axis. It is clear from the plot (bottom-right of Fig. 3) that $\Delta V_B \neq 0$ and $\Delta V_U = 0$, which can be the case if $C_U > C_B = 0$, strongly indicating that the atom is screened from the back gate by the back electron layer. Therefore the pattern of the current peak line parallel to the vertical V_B axis in the regime of high V_B and small V_F is considered as a signature that the atom is located near the front interface.

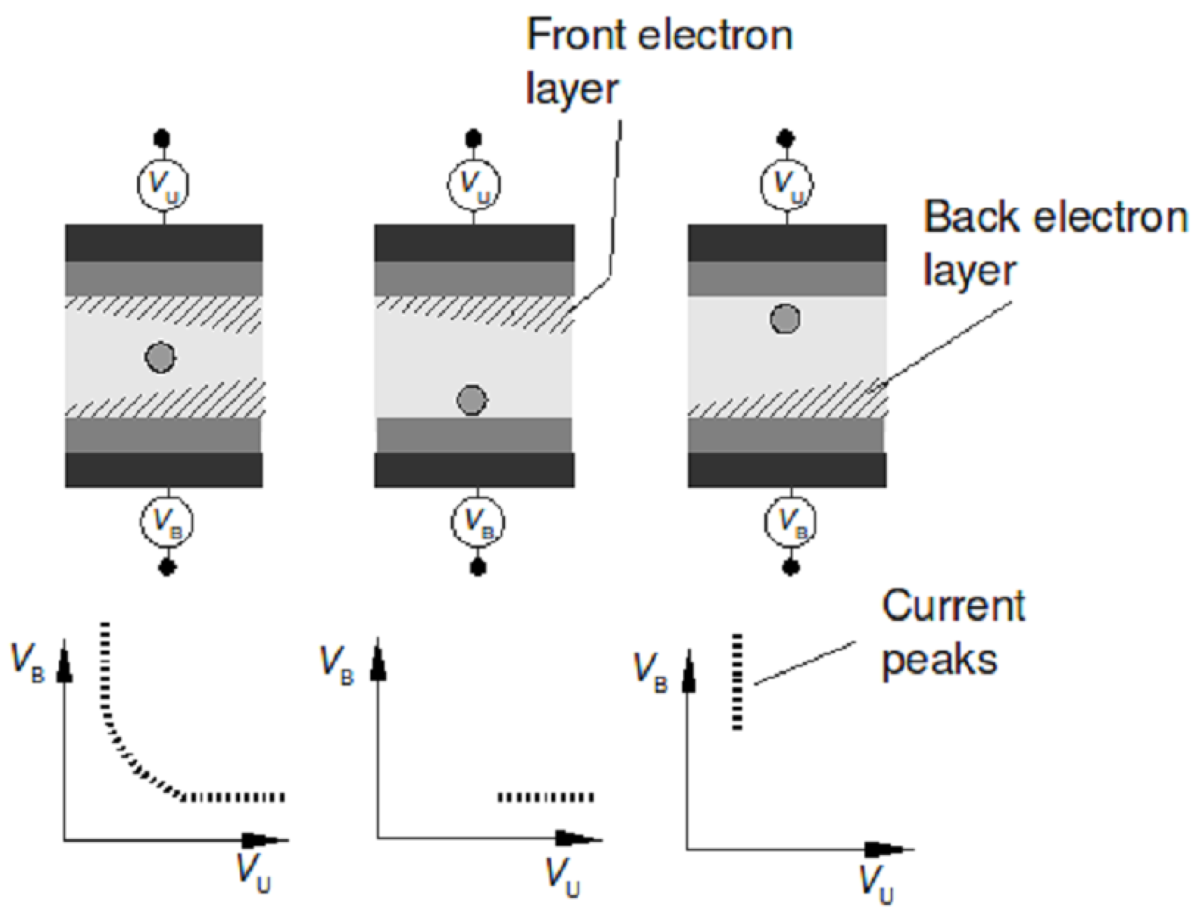

Figure 3 (top panel) the three possible depth positions of a single atom in a nano-channel section of the field effect device. The hatched regions are the electronic layers screening the atom from the gates electric fields. (bottom panel) are the tunnelling peaks (dotted lines) patterns corresponding to the configurations shown on the top panel.

5.2 Back atom

Similar arguments as that discussed in section 5.1 can be applied to the case where the atom is located near the back surface as shown in top-middle of Fig. 3. Here the back atom can be screened from the field of the upper gate by the front electron layer (hatched region, top-middle of Fig. 3) formed at large V_U and small V_B. The resulting pattern of the current peak line is shown by the dotted line in bottom-middle of Fig. 3 with slope = 0, suggesting that $C_B > C_U = 0$ because of the screening effect. Therefore the pattern of the peak line, at high V_U and small V_B, parallel to the V_U axis is a finger print for the back atom.

5.3 Middle atom

Finally, the atom near the middle of the semiconductor thickness (top-left of Fig. 3) can be screened both by the electron layer at the back surface (at large V_B and small V_U) and by the electron layer at the front surface (at small V_B and large V_U). The bottom-left of Fig. 3 shows the resulting pattern of the peak line which has two slopes, 0 (at small V_B and large V_U) and infinity (at large V_B and small V_U), caused by the screening effect from the front and back electron layers. The transition region in the pattern between these two slopes has a curvature which will not be considered in this discussion.

Conclusion

A method for identifying the depth position of an atom in a nanometer scale field effect device structure has been discussed. The depth position is identified from the pattern of the peak lines as a function of the gate voltages. Three depth positions have been identified; near the front surface, near the back surface, and near the mid-point between the back and front surface. These results have been verified experimentally by Khalafalla et al [4 5]. As a future work, we suggest computer simulation of a model of a nanometer scale field effect device to determine, using Poisson [7] and Schrödinger equations, the conduction band potential and surface electron concentration in the semiconducting active region of the device below the gate insulators. Next, a single atom can be incorporated in the active region to investigate the effect of the screening of the gates electric fields by the surface electrons on the potential of the atom.

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